AFFORDABLE EMFI ATTACKS

AGAINST MODERN IOT CHIPS

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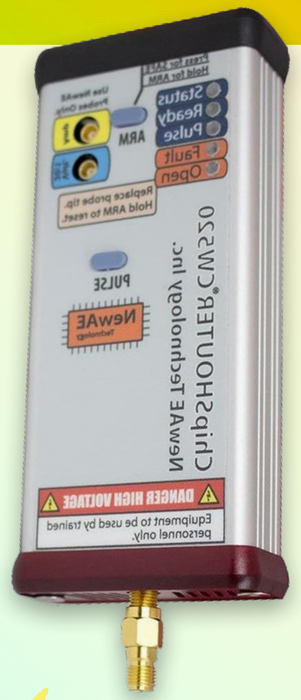
TECHNISCHE UNIVERSITÄT DARMSTADT

CRUST

AGENDA

- Motivation
- Introduction into EMFI
- Setup
- Exemplary Results



MOTIVATION

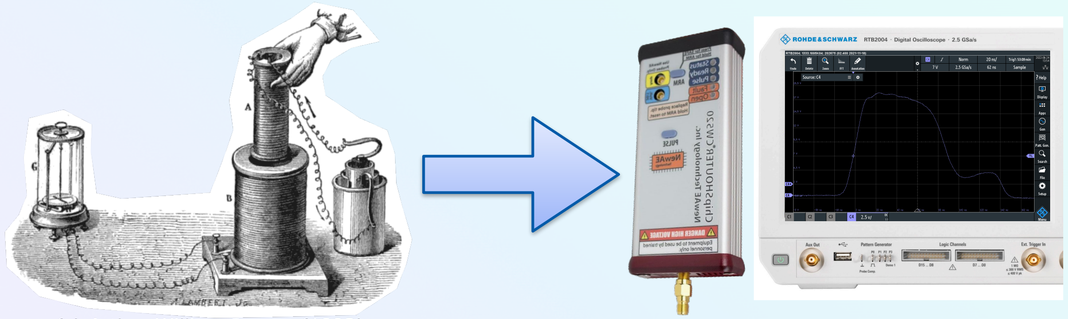
https://commons.wikimedia.org/wiki/File:Segger_J-Link_PRO.jpg

- Modern security features == classic attacks obsolete ⁉️😰
- Firmware experimentation severely limited
- Fault injection: bypass chosen instructions ➡️➡️➡️ Profit?

- Relatively new field, many devices have no countermeasures
- Tools and setup for such attacks not fully open-source / freely available / accessible

INTRODUCTION INTO EMFI

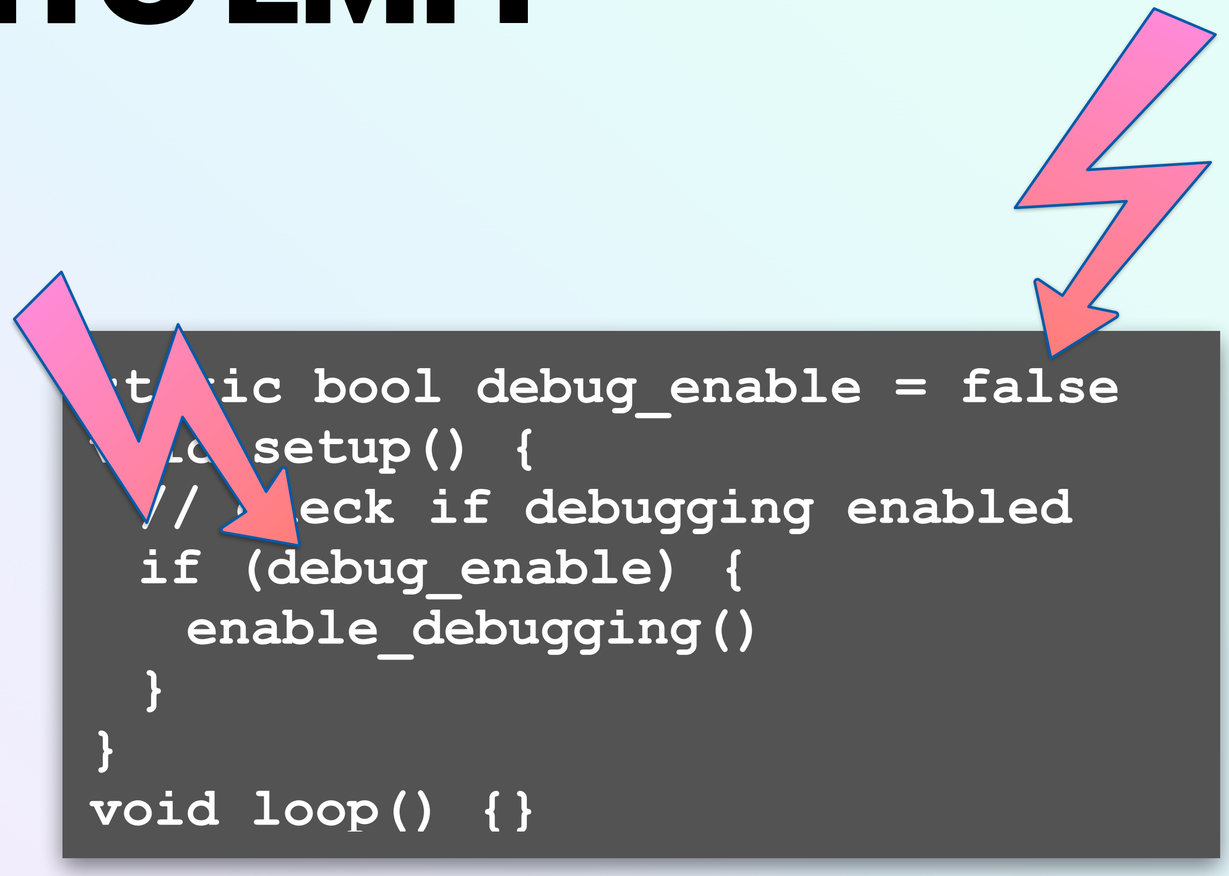
- Fault injection: introduce faults into a system to force it to behave in unintended way
- Physical FI: affect chip's internal behavior through external conditions
- 👾 EMFI: electromagnetic pulses 🧲 on SoC's and memory 👉 induce currents
  👉 affect transistor behavior
  👉 change execution path



(c) Arthur William Poyser (1892)

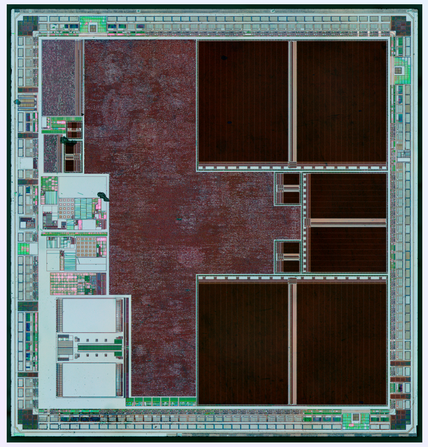
INTRODUCTION INTO EMFI

- Mitigations - if deployed at all - typically require expensive hardware changes (new revision of board / component)
- Impact of physical FI attacks is limited (require physical proximity to the target)
- However: well suited for firmware research on locked-down targets

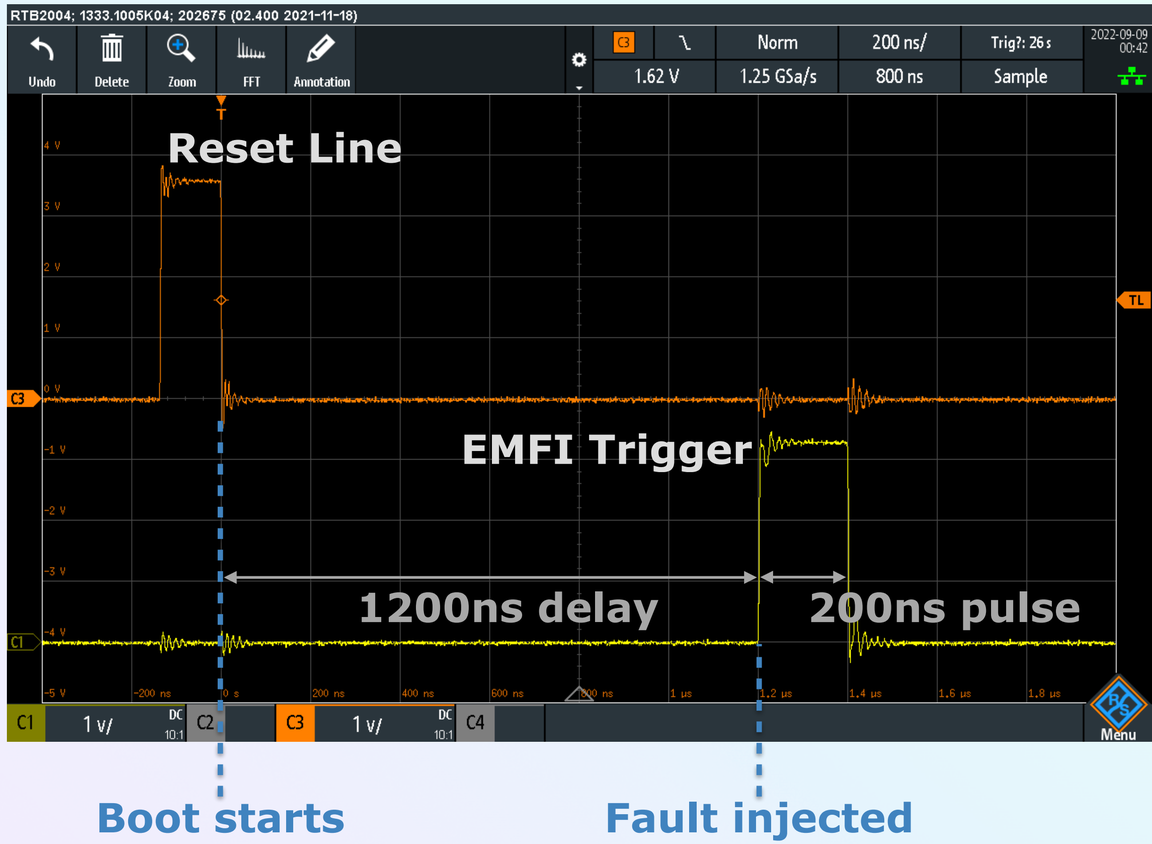


INTRODUCTION INTO EMFI

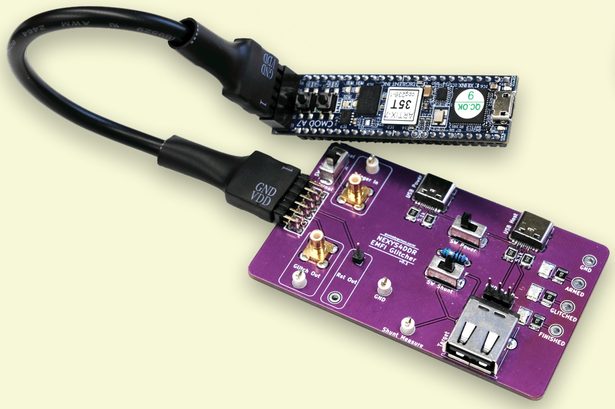
- Location & timing essential: fault exactly at the desired instruction and SoC area
- FPGA: 400MHz = 2.5ns steps
- Code, binary and power trace analysis help discover timing for potential fault

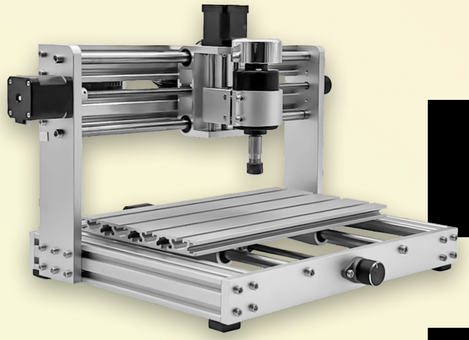


https://commons.wikimedia.org/wiki/File:GD32F103CBT6-Si-HD.jpg



EMFI SETUP 🎰



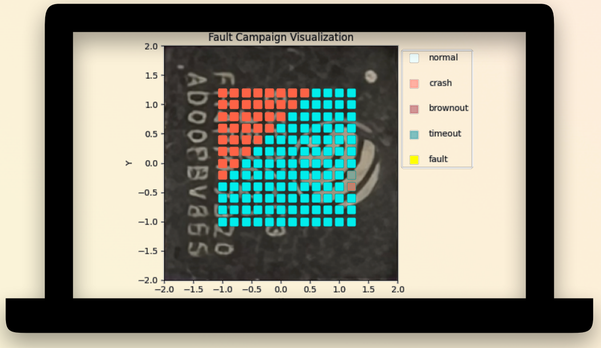


positioning platform

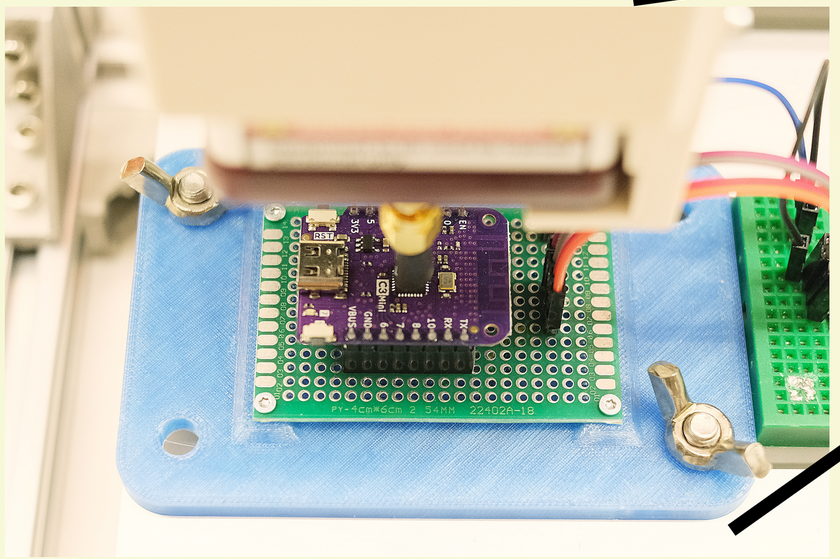
delay generator

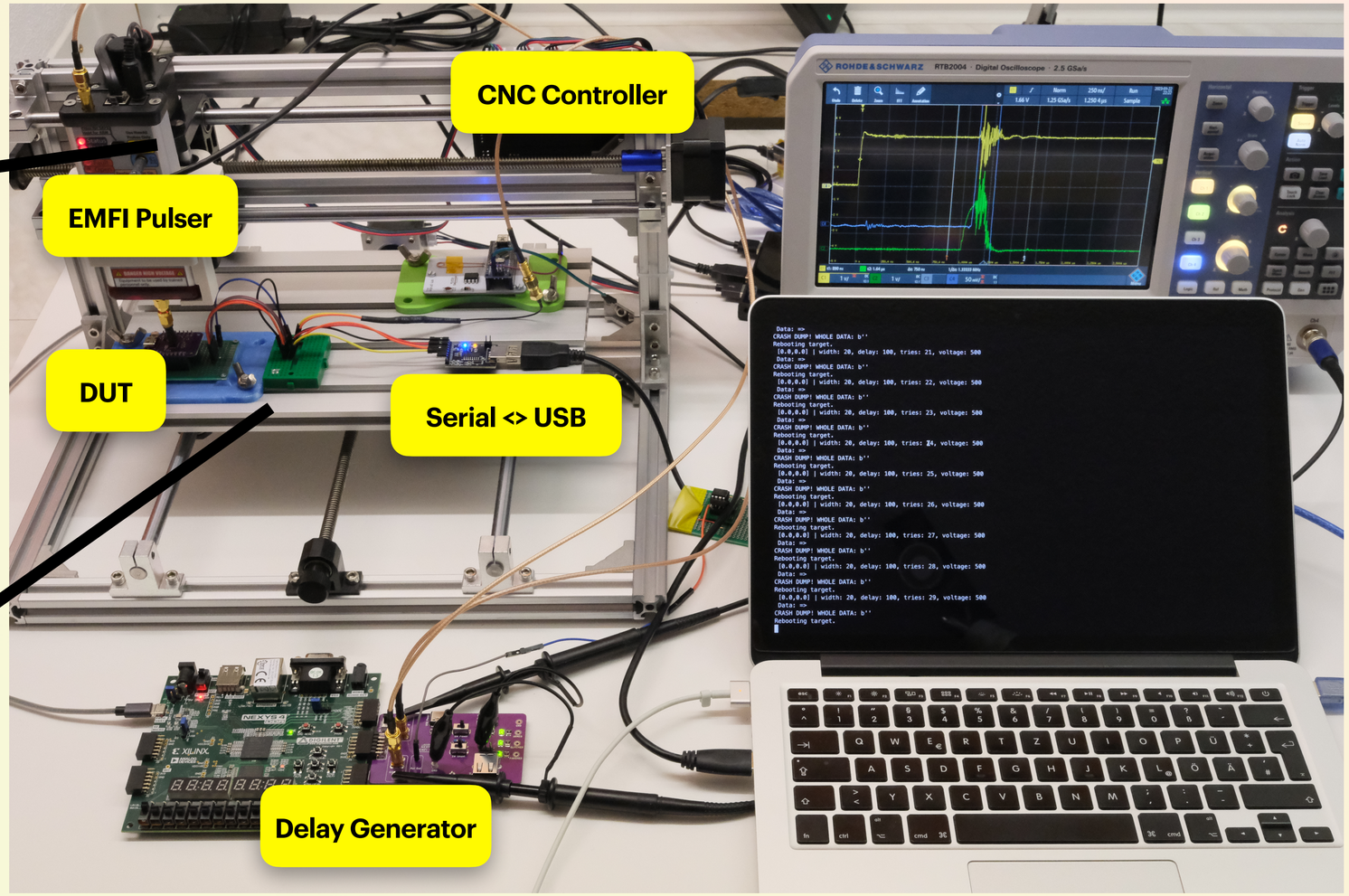
EMFI pulser

DUT



EMFI SETUP 🎰



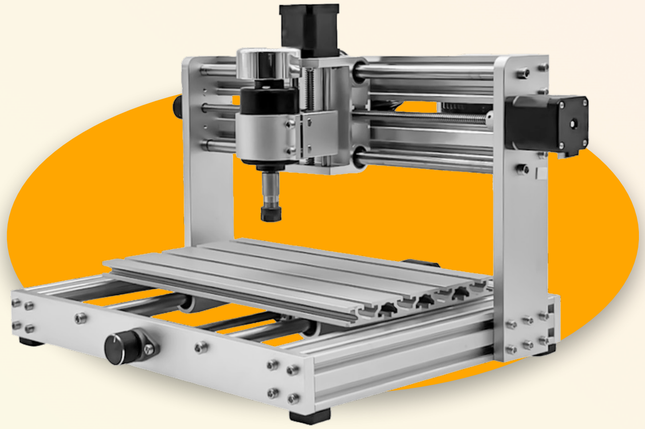


DAVIDE TOLDO | MAY 2023 | HWIO USA

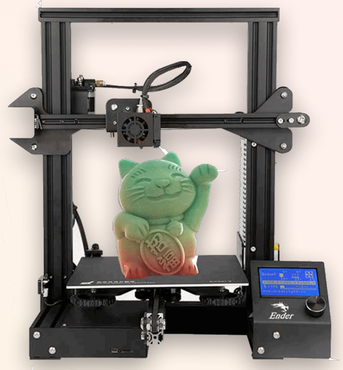
EMFI SETUP 🎰

POSITIONING PLATFORM

- CNCs or 3D printers can be used interchangeably due to GCODE
- Both are available for very low cost, come with motor controllers and everything needed
- Lead screws have approx. 10x more backlash
  ➡️ if budget allows, use belts
- Motorized XY stages offer small benefit for the price and IoT target



https://aliexpress.com



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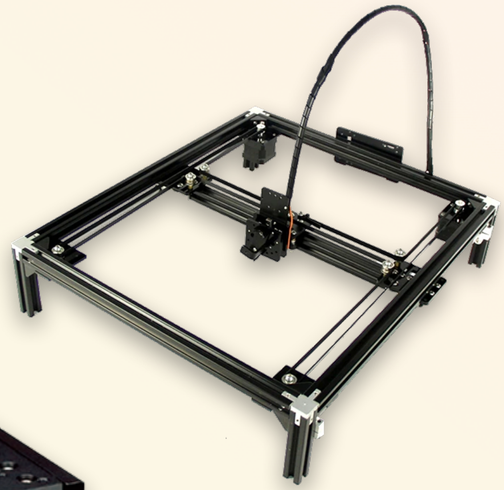

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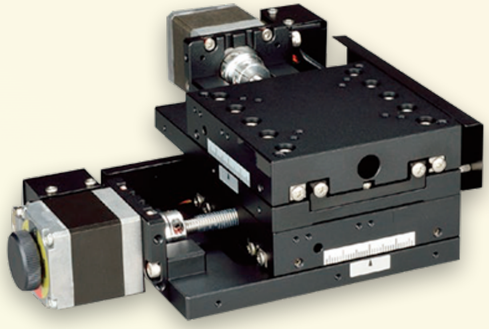
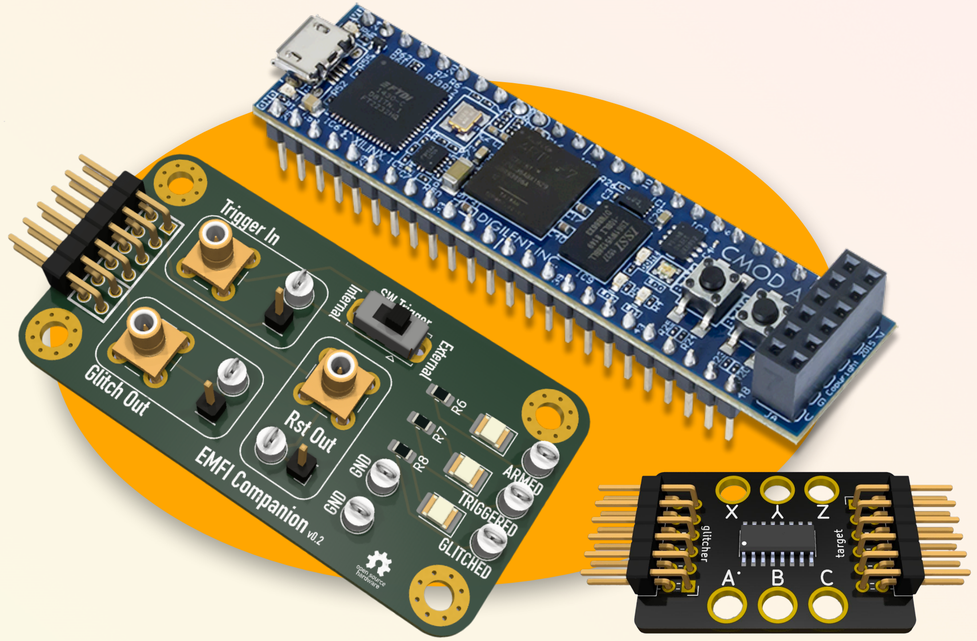


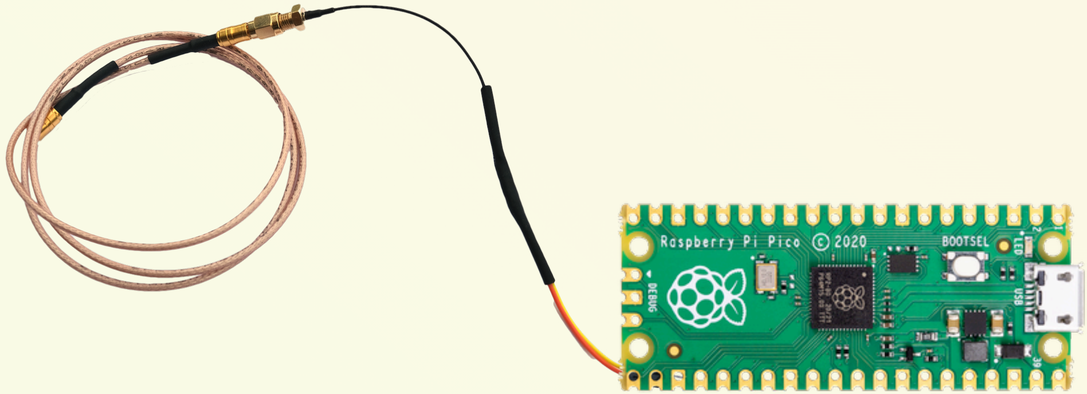
https://www.thk.com

EMFI SETUP 🎰

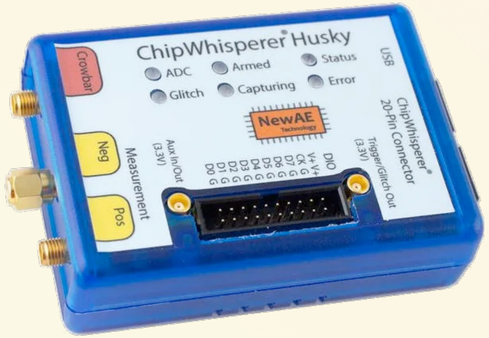
DELAY GENERATOR



- FPGA: chip.fail FOSS bitstream @stacksmashing
- Raspberry Pi Pico: custom firmware (WiP)
- ChipWhisperer @colinoflynn



https://www.raspberrypi.com/products/raspberry-pi-pico/

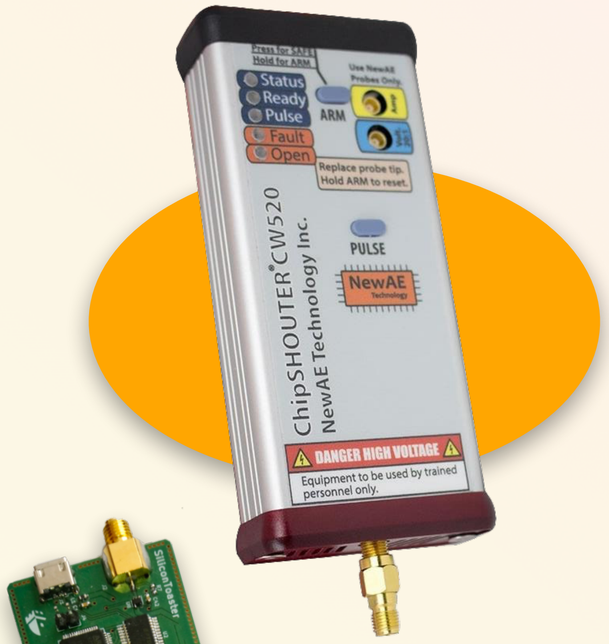


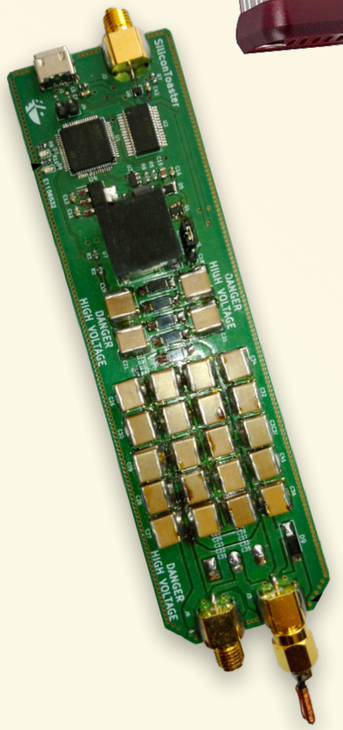
https://www.newae.com/products/NAE-CWHUSKY

EMFI SETUP 🎰

EMFI PULSER

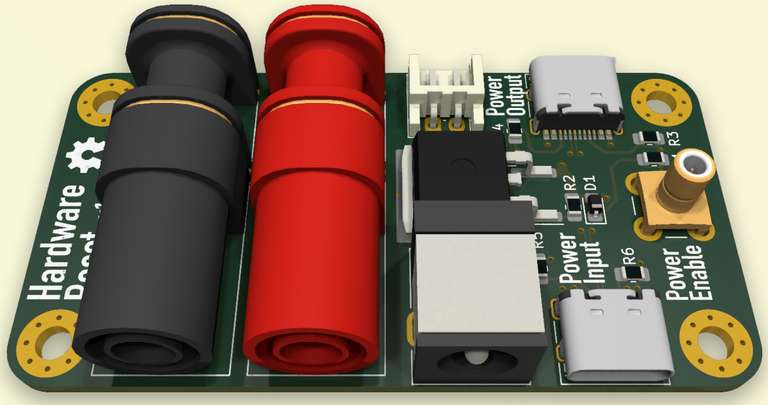
- ChipSHOUTER by @colinoflynn
- PicoEMP by @colinoflynn, @stacksmashing et al.
- SiliconToaster by Ledger



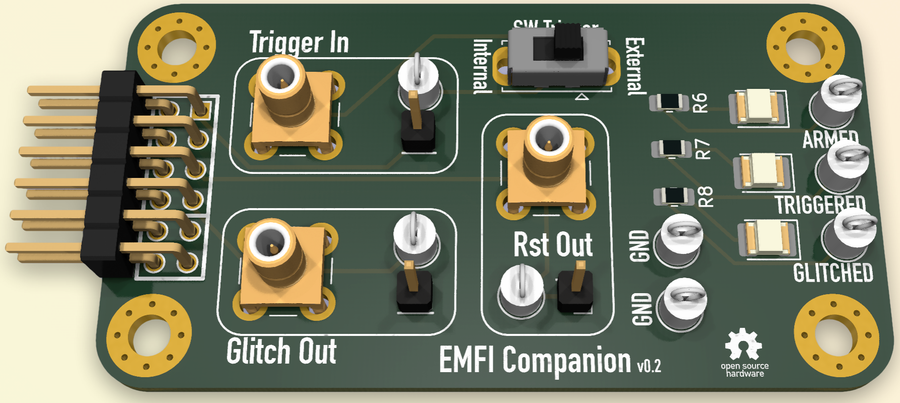


EMFI SETUP 🎰

CUSTOM HARDWARE & SOFTWARE



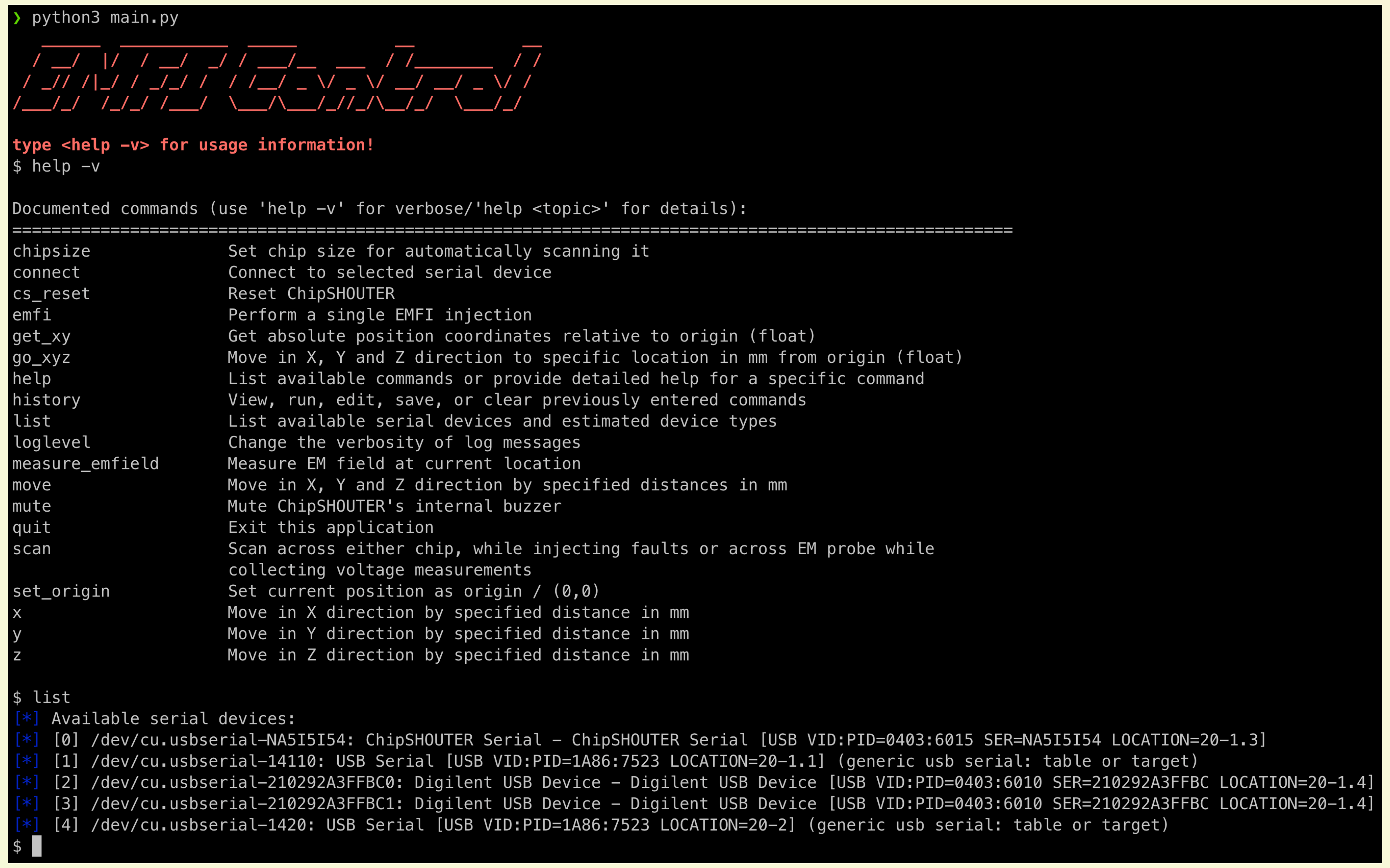
HARDWARE RESET



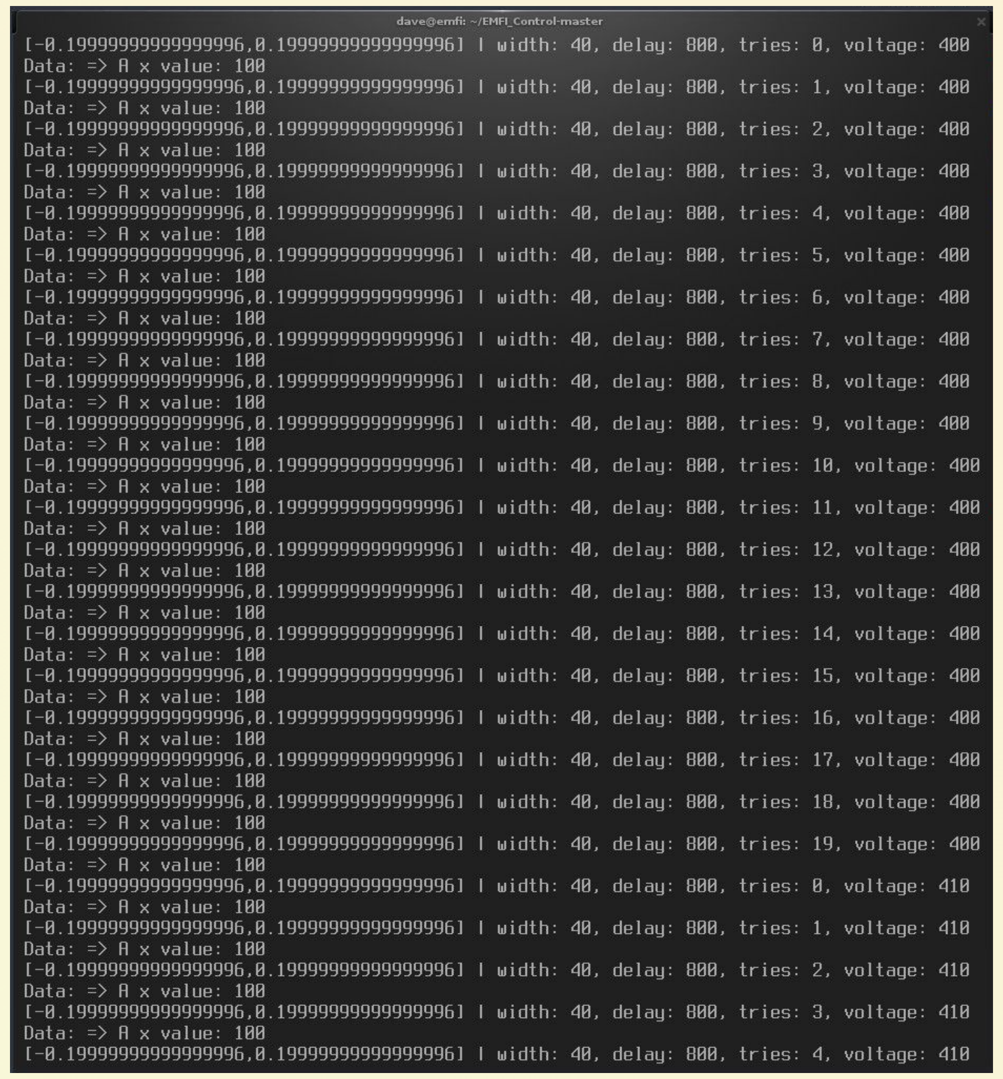
FPGA BREAKOUT

EMFI SETUP 🎰

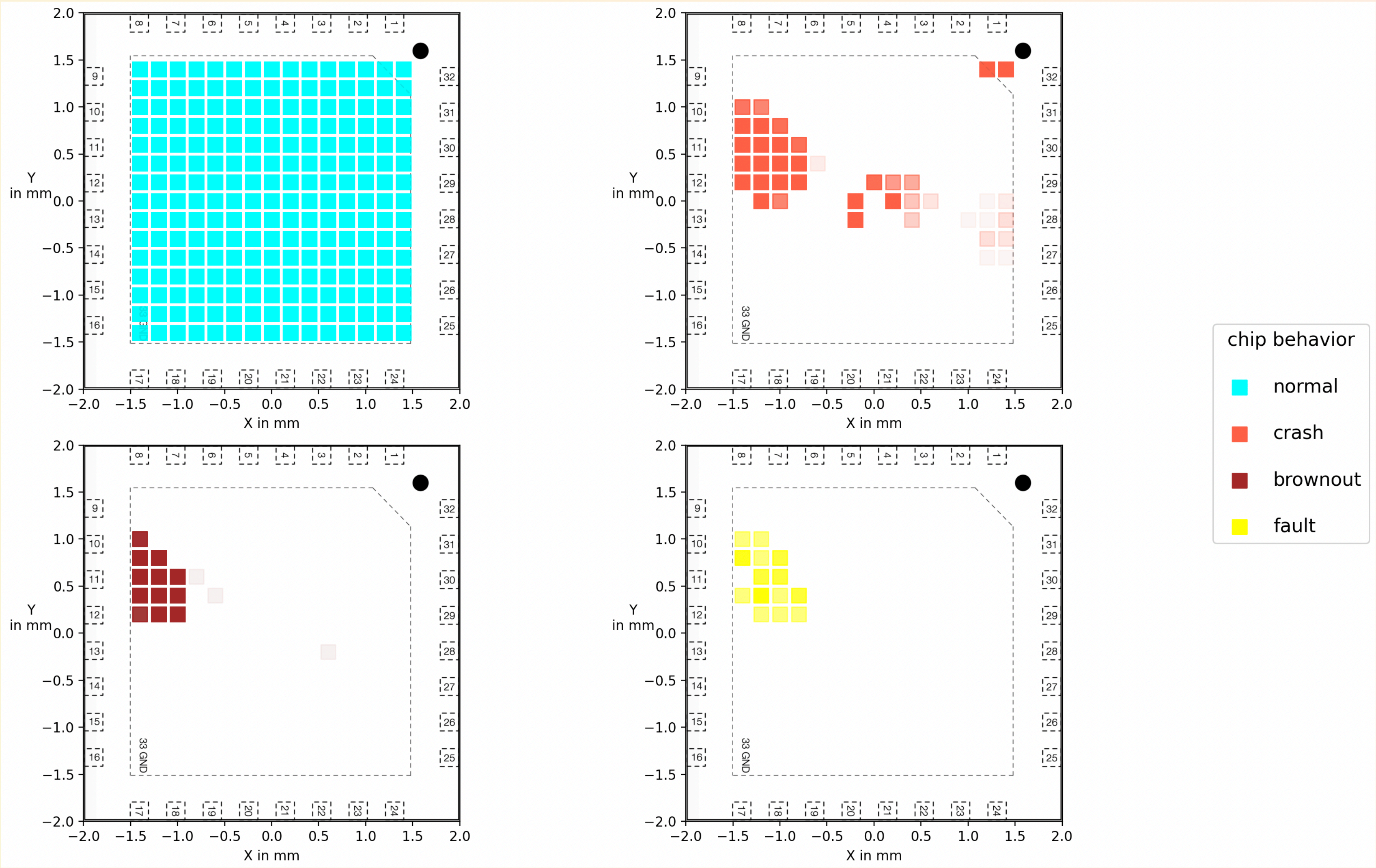
CUSTOM HARDWARE & SOFTWARE



EMFICONTROL

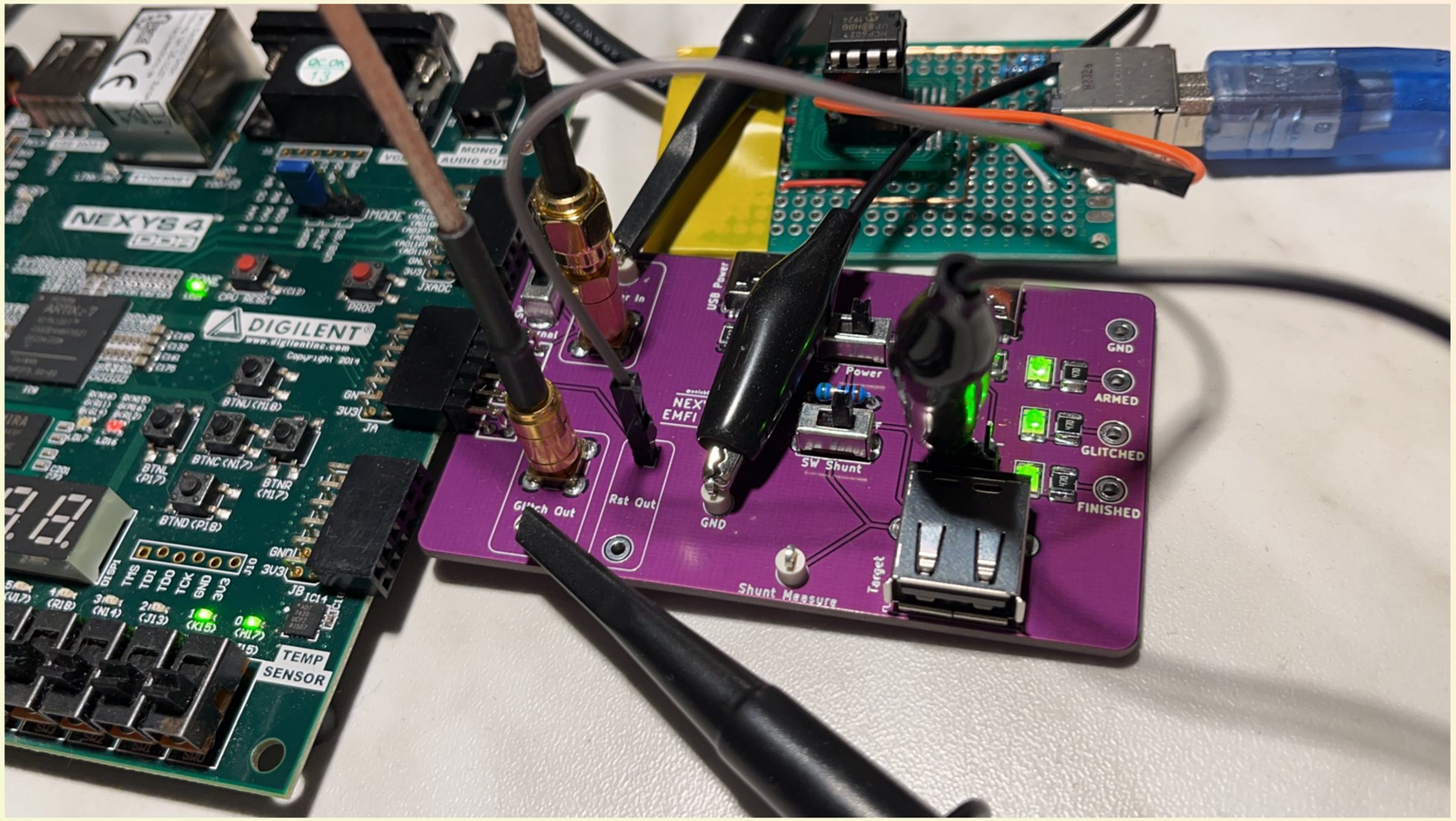


FAULT CAMPAIGN



RESULT VISUALIZATION

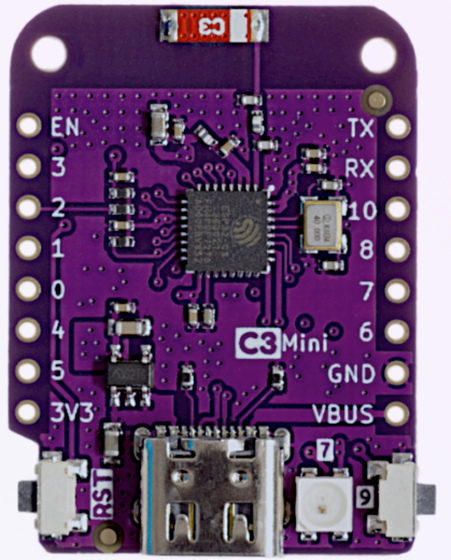
EMFI SETUP 🎰


NEXYS 4
DIGILENT
TEMP SENSOR
USB Power
Power
SW Shunt
GND
Rst Out
Shunt Measure
Target
GND
ARMED
GLITCHED
FINISHED

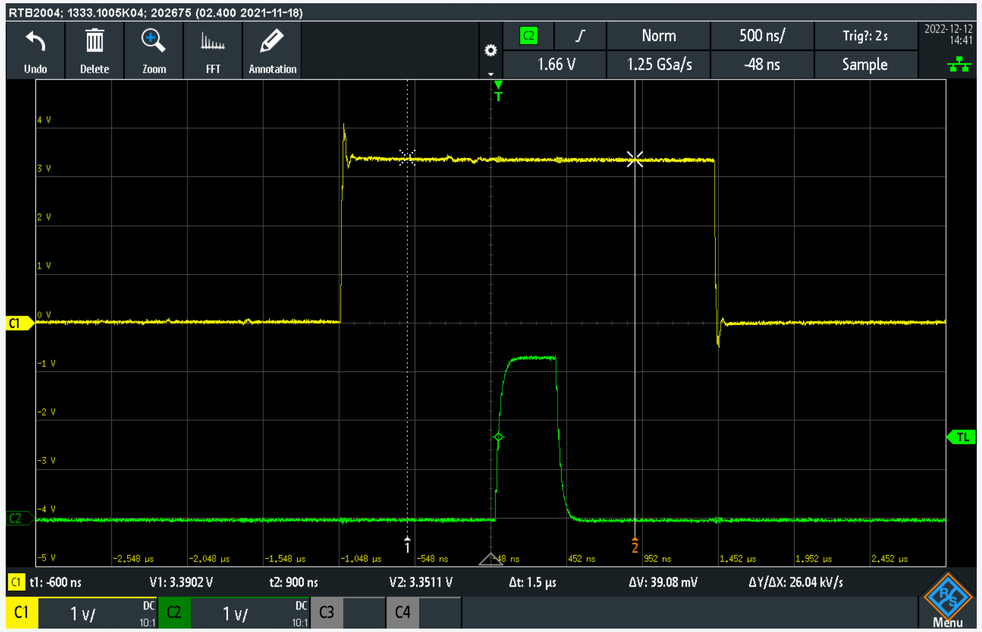
RESULTS ⁉️😐

VFI PROTECTED IOT CHIP

- Secure boot, RISC-V single core processor, no published glitching research on this version yet.



- “Simple loop” test:
  - GPIO high 👉 100 additions 👉 GPIO low 👉 check result.
  - Glitch in the middle & see if the result changes.

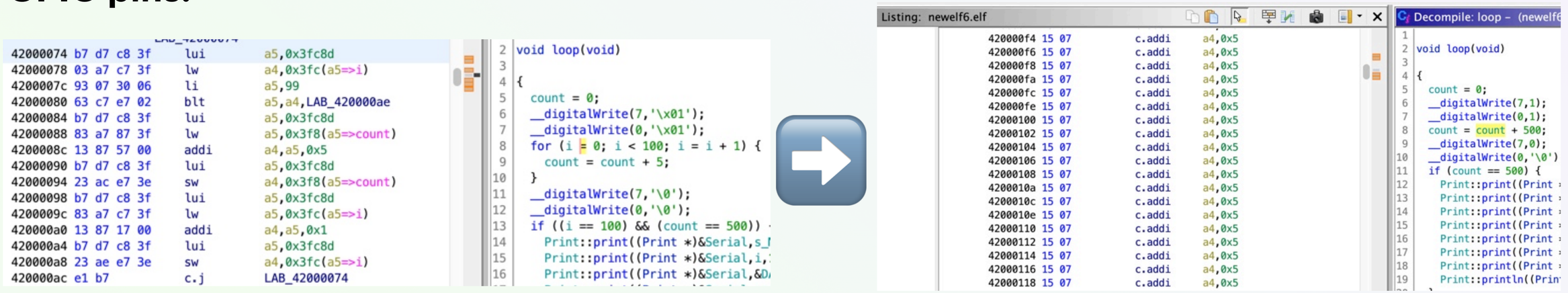


FAULT CHARACTERIZATION

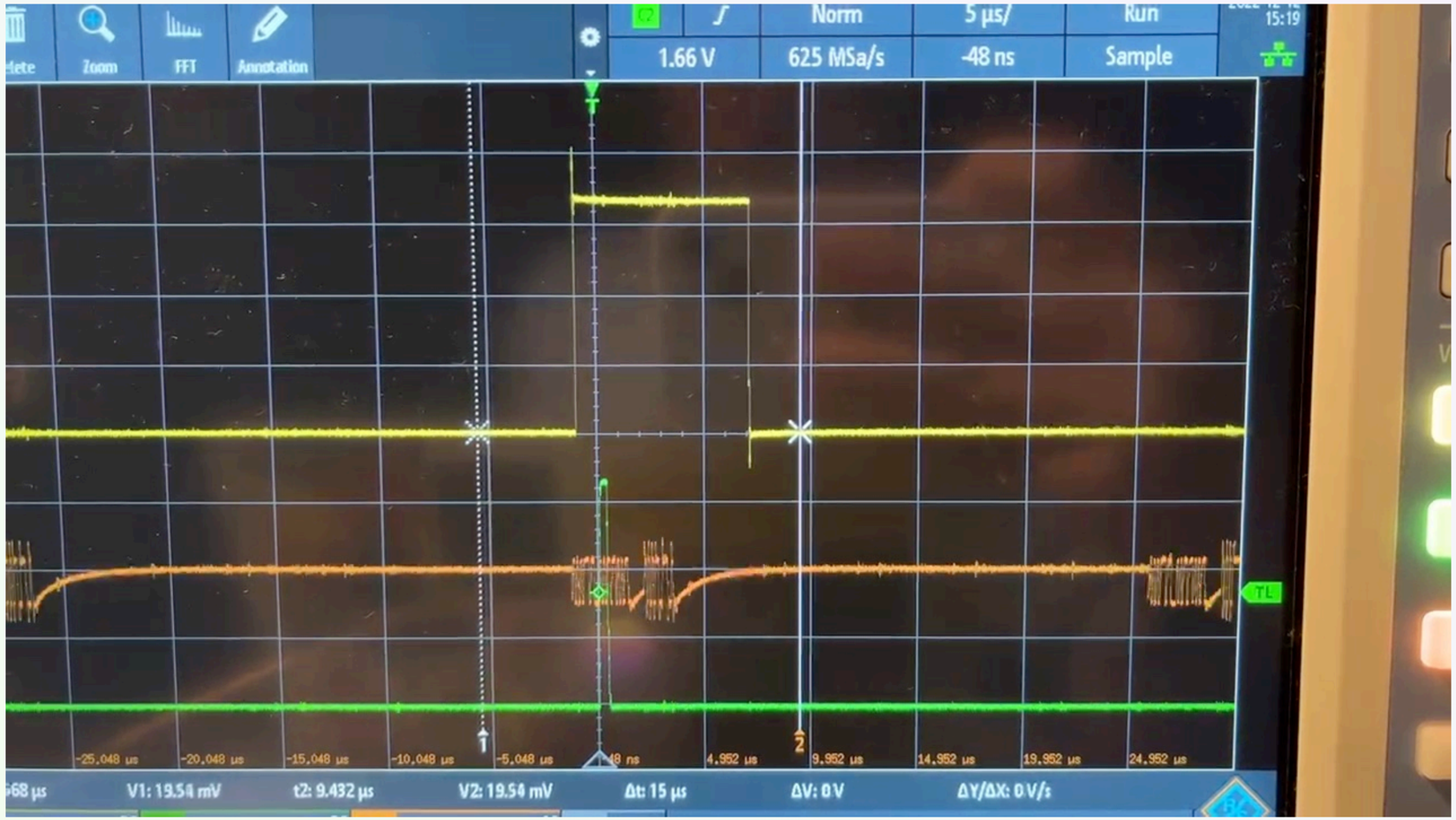
1️⃣ Toolchain compiles to FreeRTOS with brownout detection (although not dedicated for EMFI detection) and other safety checks.

2️⃣ Loop was optimized away; even without optimizations no success; so: inline assembly!

3️⃣ UART transfers corrupted by FI - switch from built-in USB-UART interface to UART via GPIO pins.



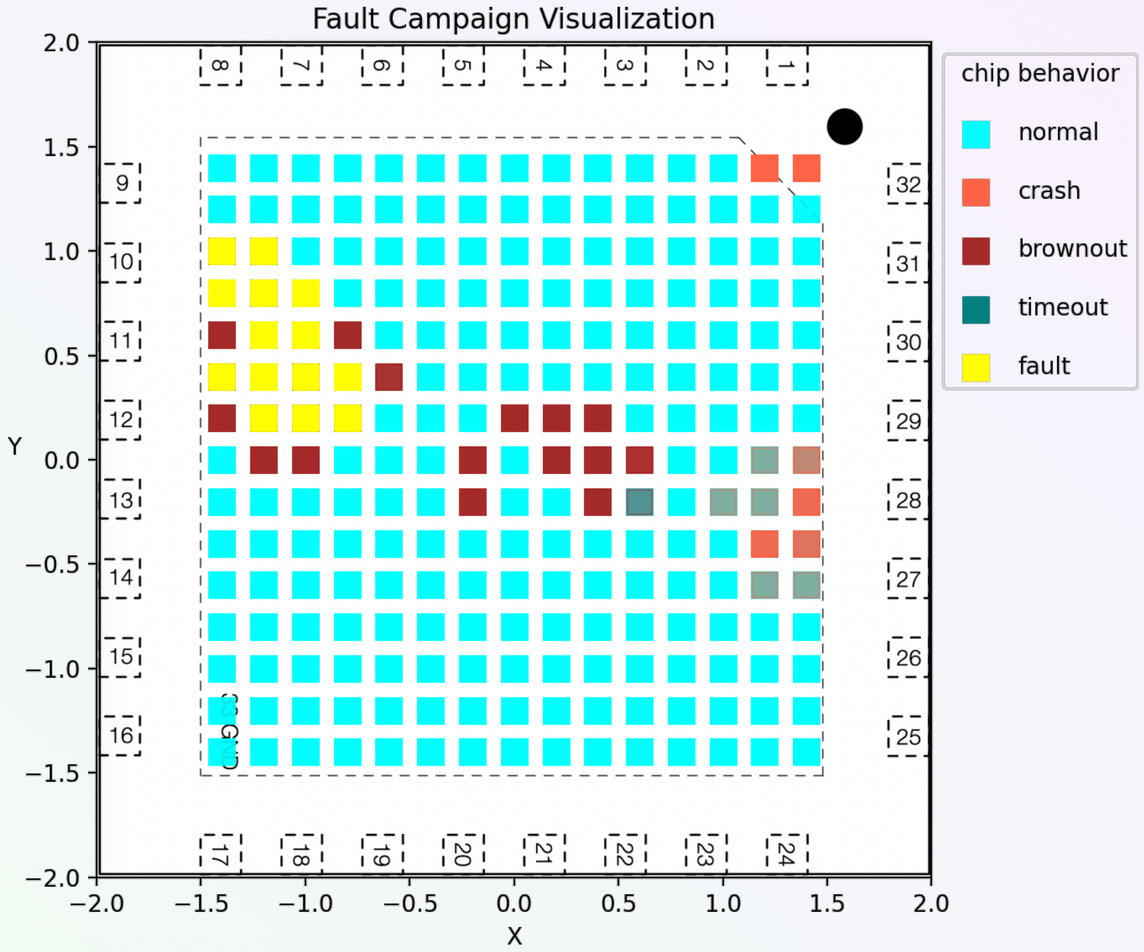
FAULT CHARACTERIZATION



FAULT CAMPAIGN

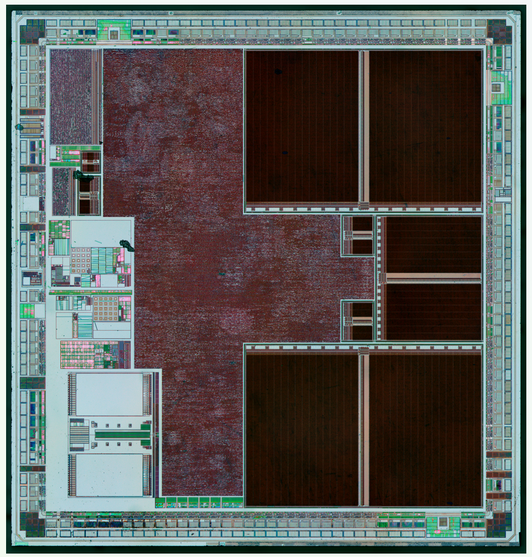
- **Successful Instruction Skip!!** 🎉🥳
- **No die-shots available, but CPU maybe in the top left?**
- **Complete top left corner is “protected” by brownout detectors.**

try_num	x	y	voltage	delay	width	normal	fault	brownout	timeout	crash	data
4	-1.0	1.0	470	100	20	FALSE	FALSE	FALSE	FALSE	TRUE	b''
5	-1.0	1.0	470	100	20	FALSE	FALSE	TRUE	FALSE	FALSE	b'dESP-ROM:esp32c3-api1-2(
6	-1.0	1.0	470	100	20	TRUE	FALSE	FALSE	FALSE	FALSE	b'No luck, try again! 100||\r\n'
7	-1.0	1.0	470	100	20	FALSE	FALSE	FALSE	FALSE	TRUE	b''
8	-1.0	1.0	470	100	20	FALSE	FALSE	TRUE	FALSE	FALSE	b'dESP-ROM:esp32c3-api1-2(
9	-1.0	1.0	470	100	20	TRUE	FALSE	FALSE	FALSE	FALSE	b'No luck, try again! 100||\r\n'
0	-1.0	1.0	480	100	20	FALSE	TRUE	FALSE	FALSE	FALSE	b'Glitch! 99||\r\n'
1	-1.0	1.0	480	100	20	FALSE	FALSE	TRUE	FALSE	FALSE	b'dESP-ROM:esp32c3-api1-2(
2	-1.0	1.0	480	100	20	FALSE	FALSE	FALSE	FALSE	TRUE	b''



FAULT CAMPAIGN

- 🕰️ Clock - related crashes in the center-right red area; proximity to oscillator.
- Die-shots 📸 could help more accurately map the SoC (requires decapping).



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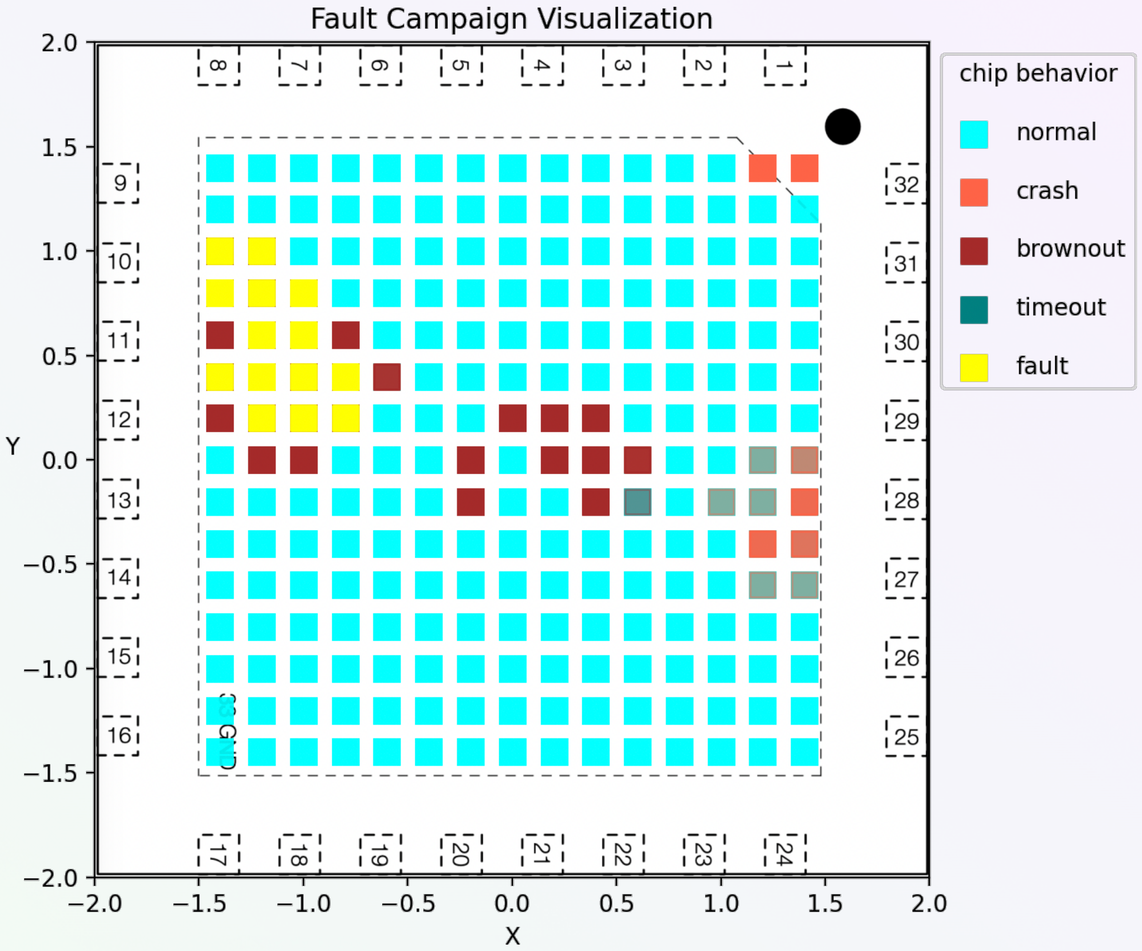
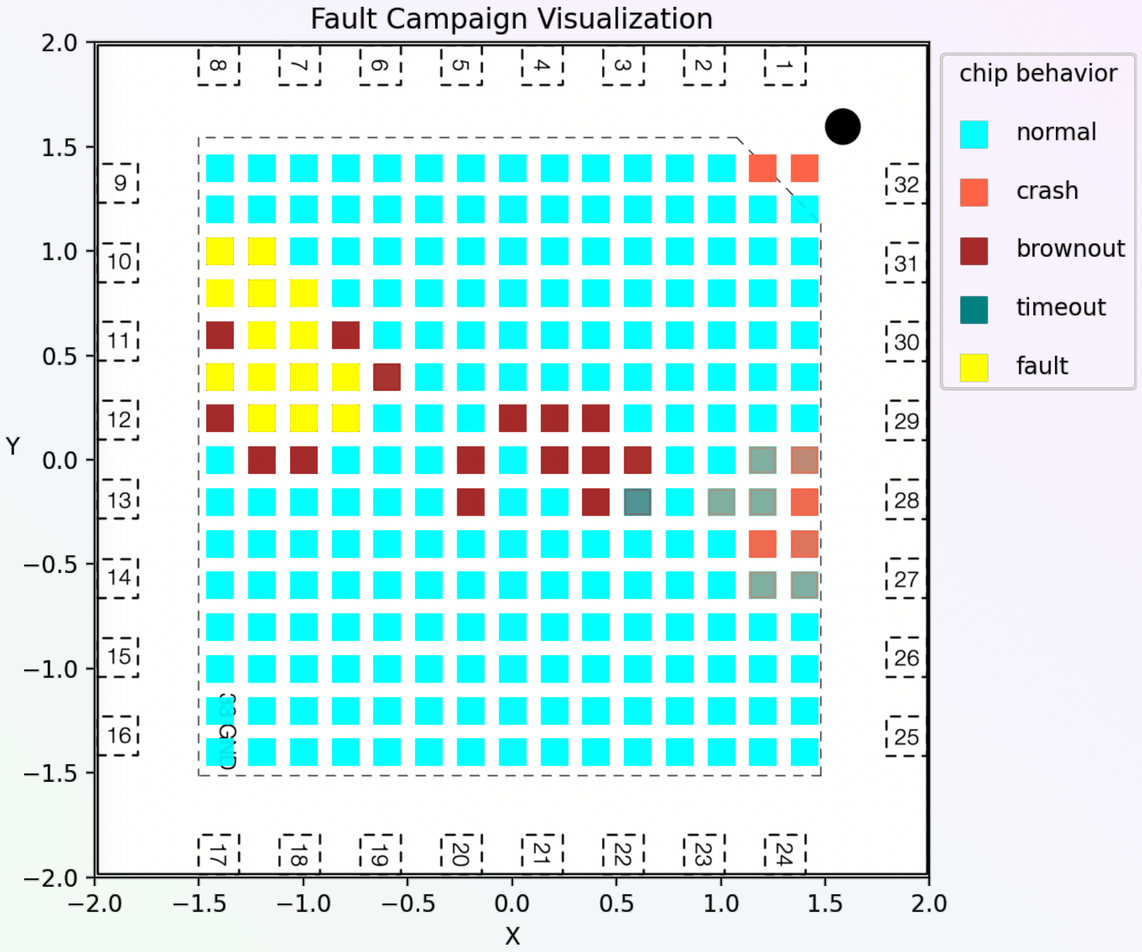


IMPACT

- "No way to fix, but... you can buy the next version 😉" - Limited Results, 2020
- Generally advanced attack, right now not reliable enough to do "in the field".
- Be aware that security features / code paths that check them can be skipped.
- Look into other chips (different architecture, maybe also more secure?)



CONCLUSION

- Low-cost, mostly FOSS / OSHW setup
  - ~$200 X-Y stage
  - ~$2000 EMFI pulser
  - ~$100 delay generator
- Can be improved with little extra cost
  - 3D printer (belts)
  - Hardware reset
  - Higher voltage pulser
- Secure against VFI, side channels, ...
  but not against serious attackers 😈

SPECIAL THANKS

- Quentin Clement 
- Philippe Teuwen 

Q&A

github.com/unixb0y/EMFI-Resources

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